I claim:

1. A method comprising:

forming oblong-shaped bumps near an edge of a first side of a first major surface of a first integrated circuit chip ("IC"), wherein a portion of each of said bumps extends beyond a perimeter of an active area of said IC and into a kerf of said IC along said first side;

removing at least a portion of said kerf along said first side thereby defining a foreshortened side of said first IC, wherein a portion of each of said bumps extends beyond an edge of said foreshortened side defining an exposed portion of said bumps;

removing at least a portion of a kerf along one side of a second IC thereby defining an foreshortened side of said second IC;

aligning an edge of said foreshortened side of said second IC with said edge of said foreshortened side of said first IC; and

attaching said first major surface of said first IC to a second major surface of said second IC, thereby defining a first level electronics package comprising a chip stack wherein:

said bumps are sandwiched between said first IC and said second IC; and

said exposed portion of said bumps extend beyond said edge of said foreshortened side of said first IC and said second IC.

2. The method of claim 1 wherein said bumps comprise metal, said step of forming oblong-shaped bumps further comprising:

forming a plurality of oblong-shaped bonding pads near said edge of said first side of said first major surface of said first IC, wherein a portion of each of said oblong-shaped bonding pads extends beyond said perimeter along said first side into said kerf;

depositing said metal on each of said oblong-shaped bonding pads; and

reflowing said metal.

3. The method of claim 2 wherein said step of removing further comprises removing at least a part of said portion of each of said oblong-shaped bonding pads that extends into said kerf.

4. The method of claim 3 wherein said step of removing comprises chemically etching said portion of said kerf and said part of said oblong-shaped bonding pads.

5. The method of claim 1 wherein said step of attaching comprises bonding said first major surface to said second major surface using adhesive.

6. The method of claim 1 further comprising joining said exposed portion of said oblong-shaped bumps of said chip stack to a second level electronics package.

7. The method of claim 6 wherein said second level electronics package is a printed circuit board.

8. A method comprising:

forming a chip stack comprising a plurality of integrated circuit chips ("ICs") that are disposed in spaced and parallel relation to one another, wherein:

said ICs are aligned with one another along an access plane;

said chip stack has a plurality of oblong-shaped bumps that are disposed between adjacent ICs in said chip stack; and

said bumps extend beyond said access plane; and

attaching said chip stack to a second level package by bonding said bumps to an array of bonding pads that are disposed on said second level package in matching locations to said bumps.

9. A high-density electronics package, comprising:

a chip stack comprising a plurality of integrated circuit chips ("IC") that are disposed in spaced and parallel relation to one another, each said IC having two major surfaces, four sides, an active device area and a kerf surrounding said active device area, wherein:

at least a portion of said kerf along one of said sides of each IC is removed defining a foreshortened side thereof;

said foreshortened side of said ICs are aligned;

a plurality of bumps are disposed along said foreshortened side between opposing major surfaces of adjacent ICs;

each said bump is disposed partially in said active device area of said IC and partially beyond an edge of said foreshortened side.

10. The high-density electronics package of claim 9 further comprising a first plurality of bonding pads that are disposed on one of said opposing major surfaces of said adjacent ICs, wherein said plurality of bumps are disposed on said plurality of bonding pads.

11. The high-density electronics package of claim 10 wherein said bonding pads are electrically connected to electrical circuitry.

12. The high-density electronics package of claim 9 further comprising adhesive that is disposed in a space between said opposing major surfaces of said adjacent ICs.

13. The high-density electronics package of claim 12 wherein said adhesive is an epoxy.

14. The high-density electronics package of claim 9 wherein said chip stack defines a first level electronics package, and further comprising a second level electronics package, wherein said second level electronics package is attached to said first level electronics package at said bumps.

15. The high-density electronics package of claim 14 wherein said second level electronics package is a printed circuit board.

16. A high-density electronics package, comprising:

a plurality of integrated circuit ("IC") chips, each said IC chip having:

electrical leads extending to one side thereof;

bonding pads disposed at said one side, wherein said bonding pads are electrically connected to said electrical leads;

bumps disposed on said bonding pads, wherein an exposed portion of each of said bumps extends beyond said one side and beyond said bonding pads; wherein:

said plurality of IC chips are secured to one another at major surfaces thereof forming a chip stack;

said one side of each said IC chip is aligned with said one side of all other IC chips in said chip stack, said aligned sides defining an access plane;

said exposed portion of each of said bumps extends beyond said access plane.

17. The high-density electronics package of claim 16 wherein said bumps have an oblong shape.

18. The high-density electronics package of claim 16 further comprising a substrate, said substrate having a plurality of electrically-conductive pads, wherein said exposed portion of said bumps is attached to said pads.

19. The high-density electronics package of claim 18 wherein said substrate comprises a printed circuit board.